AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please amend the paragraph beginning on page 1, line 17, as follows:

-- Generally, a trench is formed by etching an insulating layer, and ~~a~~ an interconnection line is formed in the trench by a self-align dual damascene process. --

Please amend the paragraph beginning on page 1, line 20, as follows:

-- In the self-align dual damascene process, a via connecting the lower and upper interconnection lines is aligned at a bottom of the trench. That is, in the self-align dual damascene process, an insulating layer is selectively etched with ~~the~~ a photolithography process to form a trench exposing a via at the bottom thereof, and a conductive layer is formed with W, Al or Cu to fill the trench. After that, ~~the~~ a portion of conductive layer outside of the trench, ~~namely a portion of the conductive layer,~~ which is not ~~necessarily~~ needed, is removed by an etching or a chemical mechanical polishing (CMP) to form ~~a~~ an interconnection line in the trench. --

Please amend the paragraph beginning on page 3, line 14, as follows:

-- Referring to Fig. 1C, a trench 21 is formed by etching the fourth interlayer insulating layer 18 using the trench mask 20. When the trench 21 is formed, the etching is stopped ~~at~~ by the etching stop layer 17. --

Please amend again the paragraph beginning on page 3, line 27, as follows:

-- As shown in Fig. 2A, after forming the trench by etching the fourth interlayer insulating layer 18, the etching stop layer 17 ~~is left~~ remains intact except at the via hole region. The etching stop layer 17 is usually formed with ~~the~~ a nitride layer having a high capacitance value, which in this case, results in a problem of a capacitance increase ~~occurs~~ due to the remaining etching stop layer 17. --

Please amend the paragraph beginning on page 4, line 10, as follows:

-- A method for forming multi-level interconnection lines using a dual damascene process is disclosed. With the dual damascene process, it is easy to control distortion of a profile ~~on~~ of a corner of a trench, and to prevent the capacitance value from increasing due to a remaining or intact etching stop layer. --

Please amend the paragraph beginning on page 5, line 5, as follows:

-- Other aspects of the disclosed methods will become apparent from the following description with reference to the accompanying drawings, ~~aherein~~ wherein: --

Please amend the paragraph beginning on page 5, line 27, as follows:

-- Referring to Fig. 3A, in a method of manufacturing multi-level metal interconnection lines, interlayer insulating layers 32 and 33 and an etching stop layer 34 are formed on a semiconductor substrate 31. After that, the etching stop layer 34 and the interlayer insulating layer 33 are selectively etched to ~~exposure~~ expose a ~~part~~ via or trench where a metal interconnection line 35 is ~~to be~~ formed. --

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Please amend the paragraph beginning on page 6, line 32 as follows:

-- Referring to Fig. 3C, after removing the via hole mask 38, another photoresist layer is coated on a resulting structure and is exposed and developed to form a photoresist pattern 40 covering the etching stop layer 37a ~~near~~ that surrounds the via hole 39 (Fig. 3B). The width d_1 of the photoresist pattern 40 is larger than that of a trench to be formed later, as much as 0.2 μm to 1.0 μm, which is a minimum size ~~of a part~~ needed ~~in an~~ for a subsequent etching process for forming an upper trench as shown in Figs. 3D and 3E. --

Please amend the paragraph beginning on page 7, line 8 as follows:

-- ~~Successively~~ Returning to Fig. 3C, the etching stop layer 37 is etched using the photoresist pattern as an etch mask to form an etching stop pattern 37a around the via hole. ~~, that is~~ That is, only the etching stop pattern 37a is left intact ~~at parts~~ where ~~an etching stop layer is needed~~ where it can be used to form an upper trench as explained later in connection with Figs. 3D and 3E. Therefore, even if the etching stop pattern 37a is formed with a layer having high dielectric constant, such as a nitrogen layer, the capacitance increase due to the relatively small portion of the etching stop pattern 37a that remains is ~~may be~~ reduced. --

Please amend again the paragraph beginning on page 8, line 4, as follows:

-- Referring to Figs. 3D and 3E, a trench is formed by etching the fourth interlayer insulating layer 41 using the trench mask 42 as an etch mask. At this time, the etching is stopped at the etching stop layer patterns 37a. The etching target may be decreased as much as the size of the void (B) generated ~~in~~ during the formation of the fourth insulating layer 41. --

Please amend again the paragraph beginning on page 8, line 19, as follows:

-- The metal interconnection lines 35 and 43 and the via 43a may be formed with any one selected from the group consisting of Al, Cu, Au, Ag and Cr. The metal layers are deposited at a thickness ranging from about 2000 Å to about 30000 Å by using any one selected the group consisting of a chemical vapor deposition (CVD), an ~~and~~ electroless deposition and a physical vapor deposition (PVD). --

Please amend again the paragraph beginning on page 9, line 5, as follows:

-- Since the ~~minimum~~ remaining portion of the etching stop layer 37a ~~for forming~~ that surrounds the trench 39 (see Figs. 3C-3E) is ~~used~~ formed by patterning the etching stop layer 37 (Figs 3B and 3C) ~~to remain in~~ so that the layer 37 remains only around the inlet of the via hole 39 (Figs. 3B and 3C), an increase ~~of~~ in capacitance due to ~~the~~ a larger remaining etching stop layer having high capacitance as shown in Figs. 2A-2B can be prevented. Also, since the interlayer insulating layer 41 having a void is etched to form the trench (Figs. 3D-3E), ~~a margin of a trench etching process may be maximized~~ the etch profile of the resulting structure shown in Fig. 3E is improved over that of the prior art structure shown in Fig. 2B. --